



Detailed Specification of 4 Bus Bar
Multicrystalline Photovoltaic Cells

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1. Mechanical Data and Design

Product	Multi-Crystalline Solar Cell based on virgin Poly-Silicon
Code	JSPL-MC-4BB-FBB1.15-RBB2.4L
Format	156 mm x 156 mm \pm 0.5 mm
Thickness	180-235 μ m
Front side (-)	Iso – textured, blue antireflective coating (silicon nitride), 4 Bus bars padded, 1.15 \pm 0.1 mm wide, 154 \pm 0.2mm length, Silver)
Back side (+)	Soldering pads, 2.4 \pm 0.2 mm wide, silver, Aluminium coated (back surface field)
Busbar distance	39 \pm 0.2 mm

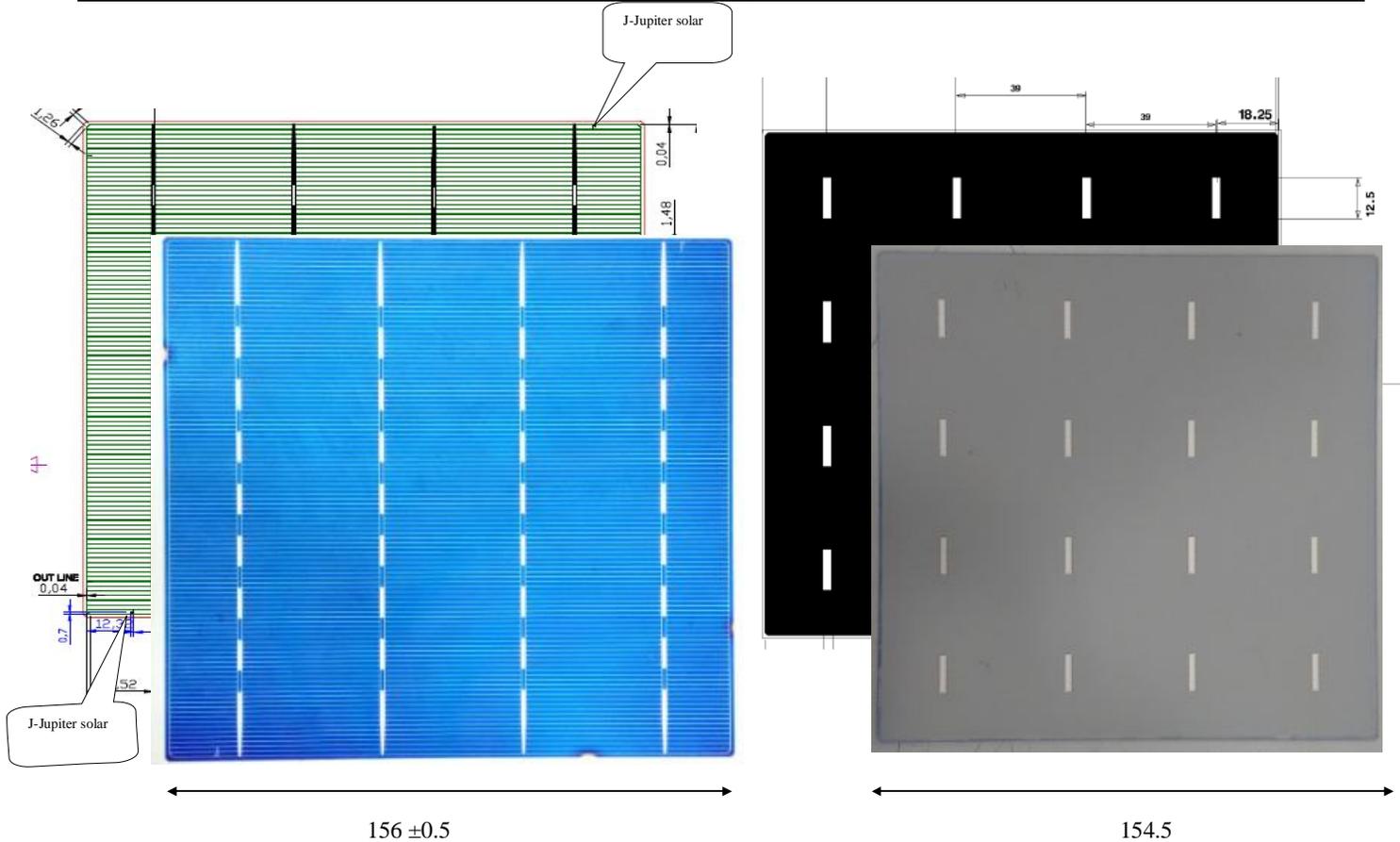
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2. Appearance

Front side of the solar cell

Back side of the solar cell



3. Electrical Performance

Efficiency Class	MC-17.00	MC-17.10	MC-17.20	MC-17.30	MC-17.40	MC-17.50
Pmpp(Wp)	4.14	4.16	4.19	4.21	4.23	4.26
Imp(A)	8.00	8.02	8.05	8.07	8.08	8.11
Vmpp(mV)	518	519	521	522	524	526

Efficiency Class	MC-17.60	MC-17.70	MC-17.80	MC-17.90	MC-18.00	MC-18.10
Pmpp(Wp)	4.28	4.31	4.33	4.36	4.38	4.40
Imp(A)	8.13	8.15	8.17	8.20	8.23	8.25
Vmpp(mV)	527	529	530	532	533	534

Efficiency Class	MC-18.20	MC-18.30	MC-18.40	MC-18.50	MC-18.60	MC-18.70
Pmpp(Wp)	4.43	4.45	4.48	4.50	4.53	4.55
Imp(A)	8.29	8.31	8.35	8.37	8.41	8.42
Vmpp(mV)	535	536	537	538	539	541

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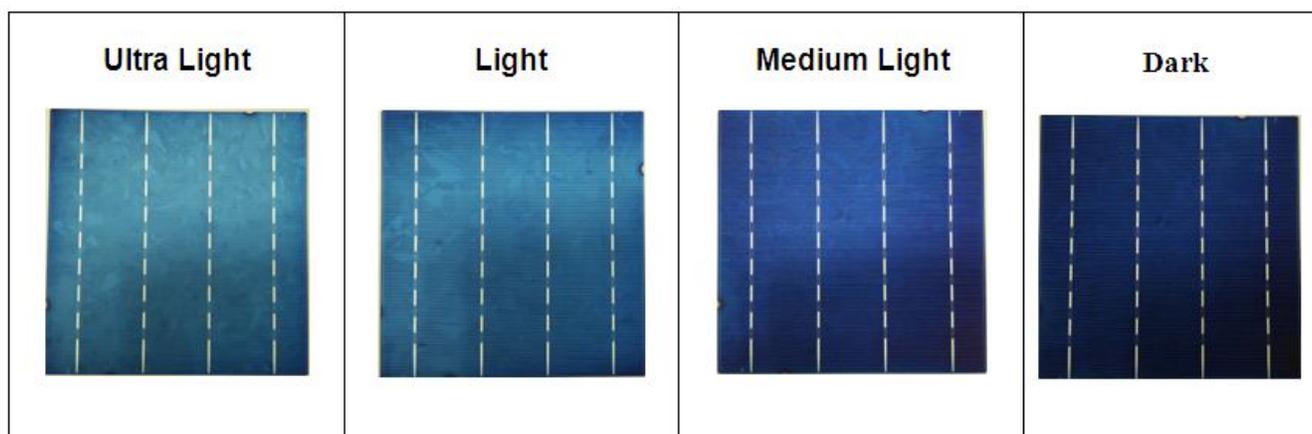
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All data measured at standard testing conditions: 1000W/m², 25°C, AM1.5G IEC 60904-3 Ed.2(2008), P_{MPP} +/-1.5 % rel. Reference cell calibrated by the Fraunhofer ISE in Freiburg

4. Cells grading & Classification

Cells classified based on

- Efficiency - minimum bin classification of 0.1% interval. For example JSPL-MC-18.00AL Class means, cell efficiency from 18.00 to 18.10%
- Shunt resistance & Leakage current at -12V criteria
- Optical appearance- i.e. Ultra Light , Light , Medium light & Dark, as below-

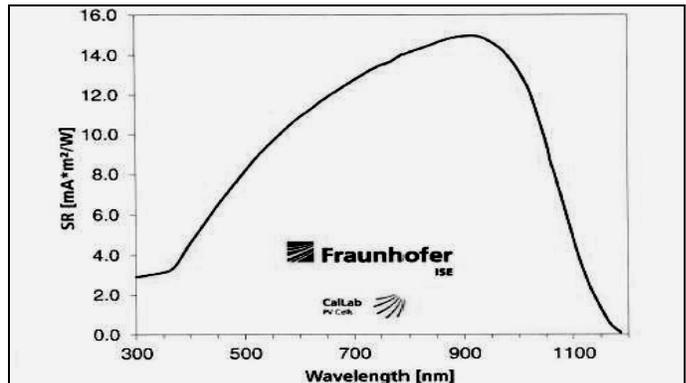
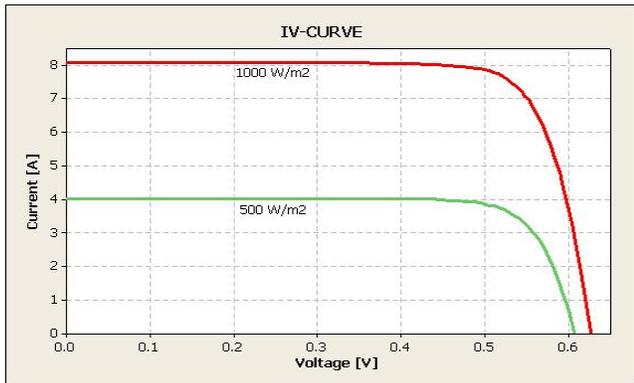


5. Behavior of electrical parameters

Temperature Coefficients		Intensity Dependence		
Power	- 0.39 %/ °C	Intensity [W/m ²]	U _{MPP} *	I _{MPP} *
Current	+0.06 %/ °C	1000	1.00	1.0
Voltage	- 0.32 %/ °C	500	0.98	0.5

*Ratio of U_{MPP} / I_{MPP} at reduced intensity to value at 1000 W/m²

6. Typical Current/Voltage-Curve and Spectral Response



7. Processing Recommendations

Solder Joint Copper ribbons coated with 16-22 µm: 62 % Sn / 36 % Pb / 2 % Ag of Thickness 250µm.

8. Reliability Test

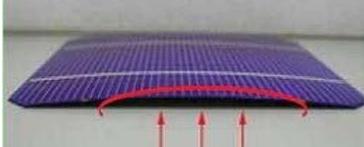
Soldering Test	Average ≥ 2.0 N & Minimum ≥ 1.0 N for FBB & RBB at 180± 3° Deg pull angle
Hot water Dip test (Back Al)	If reaction taken place within 10 - 15 min at 75 ± 5°C then failed otherwise Passed.
Tape Test(Back Al)	If Aluminium paste detached & stuck on adhesive tape then failed otherwise passed.

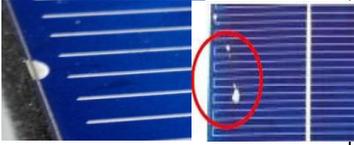
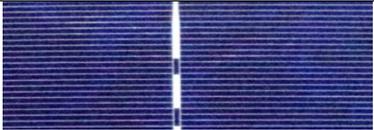
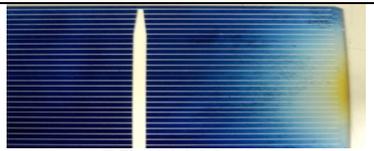
9. PID Test

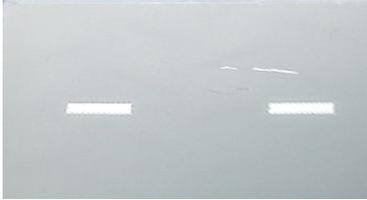
As per IEC 62804 - System voltage durability qualification test for crystalline silicon Modules- PID test at 60 °C,85%RH, 96Hrs at 1000V.

10. Visual Inspection Standard(IS 2500, Inspection Level-S3, AQL2.5)

Sr.No	Defect type	A-Grade
10.1	 V-Chip	Not Allowed
10.2	 Corner chip	Not Allowed

10.3	 Edge chip	Not Allowed
10.4	 Wafer chipping	$L \leq 0.5\text{mm}$, $W \leq 0.3\text{mm}$, $N \leq 1$
10.5	 Cracks	Not Allowed
10.6	 Visible pin hole	Not Allowed
10.7	 Bow	$H \leq 1.5\text{mm}$
10.8	 Bus bar Interruption	$L \leq 0.5\text{mm}$, $N \leq 1$
10.9	 Finger Interruption	$L \leq 1\text{mm}$, $N \leq 5$,
10.10	 Saw marks	Should not visualize
10.11	 Back Saw marks	Should not visualize

10.12	 Paste marks	Area=0.2 mm ² , N ≤ 2 Should be ≤ 2.5% in each packet
10.13	 Finger knot	L ≤ 0.3 mm, W ≤ 0.3 mm N ≤ 2 Should be ≤ 2.5% in each packet
10.14	 Strains	Area ≤ 1 mm ² , N ≤ 2
10.15	 Finger Marks	Not allowed
10.16	 Front Scratch	Visual not allowed
10.17	 Micro bubble	Should not burst
10.18	 Back Al Missing	Area ≤ 1mm ² , N≤1
9.19	 Back Busbar defects	L ≤ 2.0mm, W ≤ 1.5mm, N ≤ 1
10.20	 PECVd Marks	Not Allowed

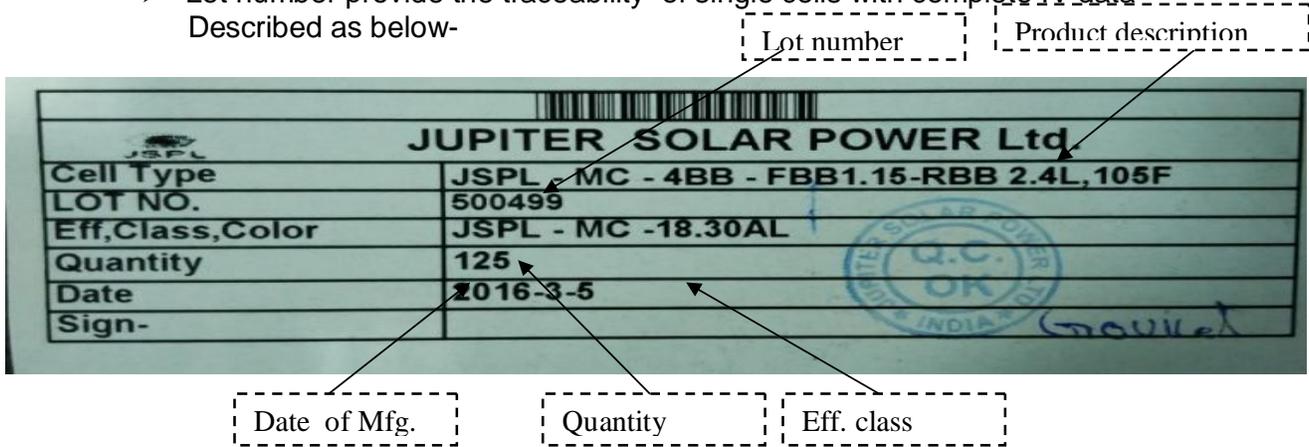
10.21	 Busbar Oxidization	Not Allowed
10.22	 Back Al Scratch	Area $\leq 1\text{mm}^2$, N ≤ 1
10.23	 Belt Mark	Should not be visualize over the entire BSF
10.24	 Colour Variation*	Not Allowed (A-grade colors samples shown below)
10.25	 Printing shift-Front	Printing Offset should not be more than $\pm 0.3\text{ mm}$
10.26	 Busbar misalignment- BackBus bar	Bus bar misalignment should not be more than $\pm 0.3\text{ mm}$
10.27	 Rotated finger layout (Disorientation relative to reference edge or wafer corner)	Should not be visualize with naked eye



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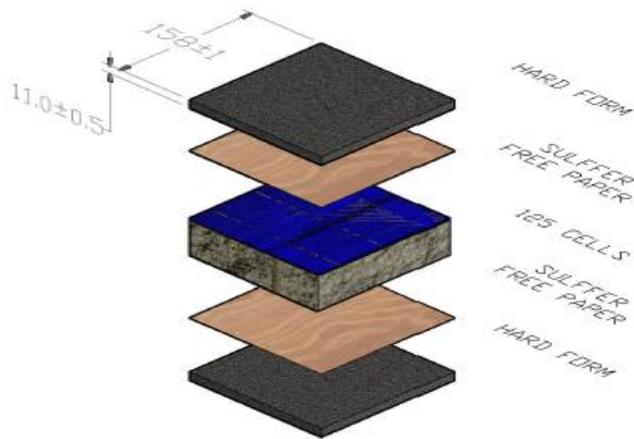
11. Product Identification & Traceability

- Every primary packing having unique lot number, Eff. class, Product description, quantity and date of manufacturing
 - Lot number provide the traceability of single cells with complete IV data
- Described as below-



12. Packing

12.1 Primary Packing

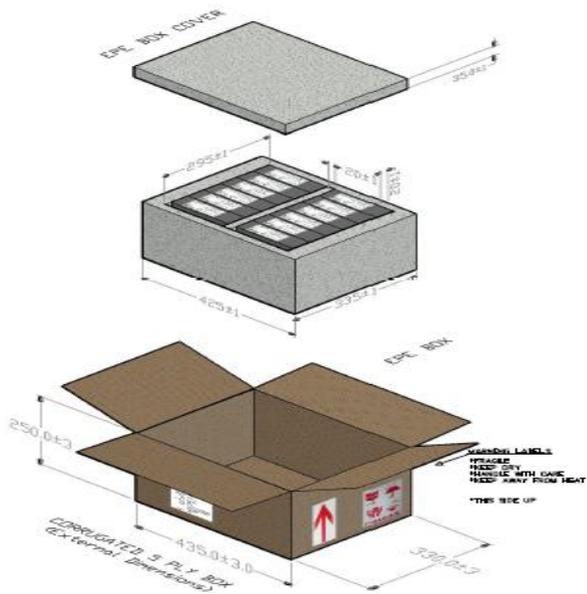


a. Comprehensive view



b. Front View

12.2 Secondary Packing



a. Comprehensive view



b. Front View

12.3 Transport Packing



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13. Storage Recommendation

Solar cells are fragile and sensitive to storage conditions. So, Cells should be stored in the situation of good airing in relative humidity $50\% \pm 5\%$ and temperature $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Solar cells are extremely susceptible to the humidity. It is recommended to make panels using the cells within the Three months of the storage period for paramount performance.

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